Appl. No. 09/673,005 Response dated June 30, 2003 Reply to Office action of February 28, 2003

## **REMARKS**

Applicant thanks the examiner for the careful examination given to the present application. The application has been reviewed in light of the Office action, and it is respectfully submitted that the application is patentable over the art of record.

Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Godbey et al. (U.S. Patent No. 5,013,681). For the following reasons, the examiner's rejection is respectfully traversed.

Godbey does not disclose or suggest a "silicon block having a surface layer delimited by a cleavage area substantially parallel to its surface" or "cleavage of the silicon block along the cleavage area to detach the surface layer fixed to the support from it" as recited in claim 1.

The Office action admits that Godbey does not explicitly teach that the silicon wafer 20 has a cleavage area parallel to its surface, but states that it would have been obvious to have such an area (Office action, 2/28/2003, page 2-3). Godbey does disclose a silicon buffer layer 22 that is used to help obtain a smooth silicon surface (col. 2, lines 39-59), and an etch stop layer that enables any remaining silicon wafer 20 and the silicon buffer layer 22 to be removed by etching (col. 4, lines 45-65). However, Godbey does not teach or suggest having a cleavage area. Therefore, Godbey does not disclose or suggest all the elements of the claimed invention.

The Office action states that Godbey discloses that the excess silicon region of the bonded silicon block is removed or cleavaged by grinding and/or polishing followed by etching operation in col. 4, lines 32-36 (Office action, 2/28/2003, page 2). As noted in the Applicant's specification, the use of a cleavage technique is known in the microelectronics field, and the Applicant's invention is a means of implementing the cleavage process in the optical field (Specification, page 4, lines 10-21). Godbey discloses that the excess silicon region 20 is removed by grinding and/or chemical polishing followed by selective etching (col. 4, lines 32-65). However, no mention is made in Godbey of using a cleavage process to detach the excess silicon region 20 from the substrate 30. Thus, Godbey does not disclose or suggest cleavage of the silicon block along the cleavage area to detach the surface layer fixed to the support. Therefore, Godbey does not disclose or suggest all the elements of the claimed invention.

Furthermore, there is no suggestion or motivation for one skilled in the art at the time the invention was made to modify Godbey to arrive at the claimed invention. Godbey discloses a

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process of producing a thin semiconductor layer by using an etch stop layer (Abstract; col. 2, lines 19-45; claim 1). The etch stop layer enables removal of any remaining silicon wafer and the silicon buffer layer by selective etching, because the etch stop layer has a different etch rate thereof. Thus, there is no motivation to modify Godbey to use a cleavage process (col. 4, lines 55-65). The desirability of using a cleavage process is found only in the Applicant's own description of the invention, in contrast to the requirement that the teaching or suggestion to make the modification must be found in the prior art, and not based on an applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Reconsideration and withdrawal of the rejection based upon Godbey is respectfully requested.

In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. 33019.

Respectfully submitted,

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Bv:

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